



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schloesser, et al. Docket No.: INF-135
 Serial No.: 10/777,128 Art Unit: 2818
 Filed: February 13, 2004 Examiner: TBD
 For: Method of Fabricating and Architecture for Vertical Transistor Cells and
 Transistor-Controlled Memory Cells

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Associate Power of Attorney

Dear Sir:

I hereby appoint as associate attorneys of record all attorneys at customer number 25962.

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Respectfully submitted,

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2004 04:40 PM

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PTO/SB/122 (06-03)

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Application Number	10/777,128
Filing Date	2/13/2004
First Named Inventor	Schloesser, et al.
Art Unit	2818
Examiner Name	TBD
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Date August 14, 2004 Telephone 972-732-1001

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